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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,145	DICKMANN, RORY	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,10-12,14 and 21* is/are rejected.

7)☒ Claim(s) *3-9,13 and 15-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/672,145 filed on 09/26/2003. Claims 1 – 21 remain pending in the application.

Specification Objections

2 The specification is objected to because of following informalities:

Page 7, Paragraph 0028, line 1, change "figure 1" to —**Figure 1**—.
Page 7, Paragraph 0029, line 1, change "figure 2 " to —**Figure 2**—.
.Page 7, Paragraph 0030, line 1, change "figure 3" to —**Figure 3**—.
Page 7, Paragraph 0031, line 1, change "figures 4a" to —**Figures 4a**—.
Page 7, Paragraph 0032, line 1, change "figure 5" to —**Figure 5**—.
Page 8, Paragraph 0033, line 1, change "figure 6" to —**Figure 6**—.
Page 7, Paragraph 0034, line 1, change "figure 7" to —**Figure 7**—.
Page 8 – 21, change "figure 1" to —**Figure 1**—.
Page 8 – 21, change "figure 2" to —**Figure 2**—.
Page 8 – 21, change "figure 3" to —**Figure 3**—.
Page 8 – 21, change "figure 4a" to —**Figure 4a**—.
Page 8 – 21, change "figure 4b" to —**Figure 4b**—.
Page 8 – 21, change "figure 5" to —**Figure 5**—.
Page 8 – 21, change "figure 6" to —**Figure 6**—.
Page 8 – 21, change "figure 7" to —**Figure 7**—.
Page 27, Abstract, line 3, change "where" to —**wherein**—.
Page 27, Abstract, line 4, before "data bus" insert —**common**—.
Page 27, Abstract, line 4, change "having" to —**comprising**—.
Page 27, Abstract, line 5, change "a group of semiconductor chip is selected" to —**selecting a group of semiconductor chips**—.
Page 27, Abstract, line 5, change "from semiconductor chips" to —**from the semiconductor chips**—.
Page 27, Abstract, line 5, change "on the base of" to —**based on**—.
Page 27, Abstract, line 7, before "data lines" delete —**the**—.
Page 27, Abstract, line 7 – 8, before "data bus" insert —**common**—.

Page 27, Abstract, line 9, change "the semiconductor... are activated" to —**activating the semiconductor chips in the selected group**—.
Page 27, Abstract, line 10, change "data interchange is performed" to —**performing data interchange**—.
Page 27, Abstract, line 10, before "data bus" insert —**common**—.

Appropriate correction is required.

Drawing Objections

3. Drawings are objected to because of following informalities:

Fig. 1 should be labeled as a —(PRIOR ART)—.
Fig. 2 should be labeled as a —(PRIOR ART)—.

Appropriate correction is required.

Claim Objections

4. Claims listed below are objected to because of the following informalities:

Claim 1, line 3, delete —**(DQ)**—.
Claim 1, line 4, change "where" to —**wherein**—.
Claim 1, line 5, before "data bus" insert —**common**—.
Claim 1, line 6, change "having" to —**comprising**—.
Claim 1, line 7, change "a group of semiconductor chip is selected" to —**selecting a group of semiconductor chips**—.
Claim 1, line 7, change "from semiconductor chips" to —**from the semiconductor chips**—.
Claim 1, line 8, change "on the base of" to —**based on**—.
Claim 1, line 9 – 10, before "data lines" delete —**the**—.
Claim 1, line 10, before "data bus" insert —**common**—.
Claim 1, line 11, change "the semiconductor... are activated" to —**activating the semiconductor chips in the selected group**—.
Claim 1, line 12, change "data interchange is performed" to —**performing data interchange**—.
Claim 1, line 12, before "data bus" insert —**common**—.

Claim 1, line 13, change "chips;" insert —**chips.**—.
Claim 2, line 2, change "where" to —**wherein**—.
Claim 2, line 2, change "chips are" to —**chip is**—.

Claim 2, line 3, change "the course" to —**a course**—.
Claim 2, line 4, change "times;" to —**times.**—.
Claim 3, line 2, change "where" to —**wherein**—.
Claim 3, line 2, before "selection" insert —**prescribed**—.
Claim 3, line 2, change "the temperature" to —**a temperature**—.
Claim 3, line 3, before "semiconductor chips" insert —**the**—.
Claim 3, line 3, change "selected;" to —**selected.**—.
Claim 4, line 2, change "where" to —**wherein**—.
Claim 4, line 2, change "method;" to —**method.**—.
Claim 5, line 2, change "where" to —**wherein**—.
Claim 5, line 2, change "the arrangement" to —**an arrangement**—.
Claim 5, line 3, change "the arrangement" to —**an arrangement**—.
Claim 5, line 4, change "components;" to —**component.**—.
Claim 6, line 2, change "where" to —**wherein**—.
Claim 6, line 3, change "data;" to —**data.**—.
Claim 7, line 2, change "where" to —**wherein**—.
Claim 7, line 2, change "probability;" to —**probability.**—.
Claim 8, line 2, change "where" to —**wherein**—.
Claim 8, line 3, after "another;" insert —**and**—.
Claim 8, line 4, change "where" to —**wherein**—.
Claim 8, line 4, before "selection probability" insert —**associated**—.
Claim 8, line 7, change "region;" to —**region.**—.
Claim 9, line 2, change "where" to —**wherein**—.
Claim 9, line 3, change "the corresponding" to —**a corresponding**—.
Claim 9, line 3, change "the position" to —**a position**—.
Claim 9, line 3 – 4, change "the corresponding" to —**a corresponding**—.
Claim 9, line 4, change "the module;" to —**the corresponding module;**—.
Claim 9, line 5, change "where the indices" to —**wherein associated indices**—.
Claim 9, line 6, change "module" to —**the modules**—.
Claim 9, line 6, after "device;" insert —**and**—.

Claim 9, line 7, change "where the indices" to **—wherein the associated indices—**.

Claim 9, line 7, change "the corresponding" to **—a corresponding—**.

Claim 9, line 9, change "indices;" to **—associated indices.—**.

Claim 10, line 2, change "where" to **—wherein—**.

Claim 10, line 3, change "up;" to **—up.—**.

Claim 11, line 2, change "where" to **—wherein—**.

Claim 11, line 3, change "where method" to **—wherein the method—**.

Claim 11, line 3, before "content" delete **—the—**.

Claim 11, line 4, change "redundant;" to **—redundant.—**.

Claim 12, line 2, change "where" to **—wherein—**.

Claim 12, line 3, change "where the data" to **—wherein data—**.

Claim 12, line 4, change "step a);" to **—step a).—**.

Claim 13, line 2, change "where" to **—wherein—**.

Claim 13, line 5, before "data bus" insert **—common—**.

Claim 13, line 6, change "where" to **—wherein—**.

Claim 13, line 6, before "data bus" insert **—common—**.

Claim 13, line 7, change "a group" to **—the group selected—**.

Claim 13, line 7 – 8, change "the groups of semiconductor chips;" to **—groups of semiconductor chips.—**.

Claim 14, line 1, before "semiconductor chips" insert **—operating—**.

Claim 14, line 3, change "where" to **—wherein—**.

Claim 14, line 4, change "data bus;" to **—common data bus, comprising—**.

Claim 14, line 5, change "where a selection device is designed in order to select" to **—a selection device for selecting—**.

Claim 14, line 6, change "the group" to **—a group—**.

Claim 14, line 6, change "on the base of" to **—based on—**.

Claim 14, line 8, change "where an activation device is designed in order to activate" to **—an activation device for activating—**.

Claim 14, line 9, before "data lines" delete **—the—**.

Claim 14, line 9, change "data bus;" to **—common data bus.—**.

Claim 15, line 2, change "where" to **—wherein—**.

Claim 15, line 2, change "in order to select" to **—for selecting—**.

Claim 15, line 3, change "the active" to **—an active—**.

Claim 15, line 3, change "on the base of the temperature" to **—based on a temperature—**.
Claim 15, line 3, change "chips;" to **—chips.—**.
Claim 16, line 2, change "where" to **—wherein—**.
Claim 16, line 2, change "in order to select" to **—for selecting—**.
Claim 16, line 3, change "the active" to **—an active—**.
Claim 16, line 3, change "method;" to **—method.—**.
Claim 17, line 2, change "where" to **—wherein—**.
Claim 17, line 2, change "in order to assign" to **—for assigning—**.
Claim 17, line 2, change "each semiconductor chip" to **—each of the semiconductor chips—**.
Claim 17, line 3, change "on the base of " to **—based on—**.
Claim 17, line 4, change "chips;" to **—chips.—**.
Claim 18, line 1, after "claim 14," insert **—further comprising—**.
Claim 18, line 2, change "where an assessment device is designed in order to access" to **—an assessment device for accessing—**.
Claim 18, line 3, change "the temperature" to **—a temperature of the semiconductor chips—**.
Claim 18, line 4, change "where" to **—wherein—**.
Claim 18, line 4, change "where the selection device is designed in order to select" to **—wherein the selection device is designed for selecting—**.
Claim 18, line 4 – 5, change "on the base of the" to **—based on—**.
Claim 18, line 5, change "the assessment results" to **—assessment results—**.
Claim 18, line 5, change "device;" to **—device.—**.
Claim 19, line 2, change "where" to **—wherein—**.
Claim 19, line 2, change "in order to activate" to **—for activating—**.
Claim 19, line 3, change "the active group" to **—an active group—**.
Claim 19, line 3 – 4, change "each semiconductor chip" to **—each of the semiconductor chips—**.
Claim 19, line 4, change "the corresponding" to **—a corresponding—**.
Claim 19, line 4 – 5, change "the position of the corresponding semiconductor chip;" to **—a position of a corresponding semiconductor chip.—**.
Claim 20, line 1, after "claim 14," insert **—further comprising—**.

Claim 20, line 2 – 3, change "where a register device is designed in order to store the information about the association" to **—a register device for storing information about an association—**.

Claim 20, line 3 – 4, change "the active group of semiconductor chips; " to **—an active group of the semiconductor chips.—**.

Claim 21, line 3, change "where" to **—wherein—**.

Claim 21, line 4, change "data bus;" to **—common data bus, comprising—**.

Claim 21, line 5, delete **—having—**.

Claim 21, line 5, before "data lines" delete **—the—**.

Claim 21, line 6, before "data bus" insert **—common—**.

Claim 21, line 6, change "comprising" to **—including—**.

Claim 21, line 6, delete **—the purpose of—**.

Claim 21, line 7, before "memory chips" insert **—the—**.

Claim 21, line 7, before "data bus" insert **—common—**.

Claim 21, line 7 – 8, change "on the base of" to **—based on—**.

Claim 21, line 9, delete **—the purpose of—**.

Claim 21, line 9 – 10, change "selected group for data exchange" to **—selected group of the memory chips for the data interchange—**.

Claim 21, line 10, change "data bus;" to **—common data bus; and—**.

Claim 21, line 11, delete **—having—**.

Claim 21, line 11, delete **—the purpose of—**.

Claim 21, line 11, before "data" delete **—the—**.

Claim 21, line 12, change "the group of memory chips" to **—the selected group of the memory chips—**.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 10 – 12, 14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,438,014 B2 to *Funaba et al.* in view of U.S. Patent No. 6,209,074 B1 to *Dell et al.*

7. As to Claims 1 and 14, *Funaba et al.* shows and disclose the following subject matter:

- A plurality of *memory chips* (i.e., *semiconductor chips*) are arranged in groups on *memory modules* which are connected to a common *memory access data bus* , wherein each memory chip on each memory module is connected to at least one data line in the common *memory access data bus* – [Fig. 11; Fig. 14; Fig. 1; abstract; col. 1, line 34 – 45; col. 3, line 21 – 52];
- memory chips on one memory module are selected using an associated *chip select signal* generated by a *memory controller* – [col. 1, line 38 – 40]; Notice that a group of memory chips in the memory modules can be selected using associated chip select signals;
- The memory chips in the selected group use data lines over the entire bus width of the memory access data bus – [col3, line 21 – 32; col. 9, line 19 – 20];
- Each memory chip in the selected group is activated by RAS (row address strobe), CAS (column address strobe), and DQSL and DQSU, which are data access command signals– [col. 9, line 34 – 38]; Notice that (1) the RAS, CAS, DQSL and DQSU are *memory chip activation commands* (2) after receiving the *memory chip activation commands*, data exchange can be performed between data lines in the memory access data bus and the selected group of memory chips.

Funaba et al. do teach selecting a group of memory chips based on a prescribed *selection criterion* independently of module. But *Dell et al.* teach applying an advanced *selection criteria* in selecting an *optimal number of memory chips* in different memory modules in order to achieve an optimal memory bank which is compatible with a variety of computer systems having different performance requirements – [col. 1, line 16 – 17; col. 2, line 22 – 37; col. 3, line 35 – 54]. Notice that, when applying the advanced *selection criterion*, the memory chips are selected independently of module.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Dell et al.* teach applying an advanced *selection criteria* in selecting an *optimal number of memory chips* in different memory modules in order to achieve an optimal memory bank which is compatible with a variety of computer systems having different performance requirements.

For reference purposes, the explanations given above in response to Claims 1, 14 and 21 are called **[Response A]** hereinafter.

8. As to Claim 2, as explained in **[Response A]** given above, *each memory chip* is being a member of the selected group should go through two separate steps, namely selection step and activation step. Each step takes on cycle. Therefore method steps)a to)c are repeated and different memory chip is selected in a course of two cycles taking place at successive times.

9. As to Claim 10, *Dell et al.* show and teach the subject matter (power on reset, address re-map et al.) in Fig. 2.

10. As to Claims 11 and 12, *Funaba et al.* teach subject matter regarding *semiconductor chips* are *memory chips* in **[Response A]**. *Dell et al.* show and teach temporarily saving content of memory chips (to memory storage) before remapping the memory chips – [Fig. 2]. Notice that, after storing the content of the memory chips as a back-up, the content the memory chips become redundant.

For reference purposes, the explanations given above in response to Claims 11, 12 and 21 are called **[Response B]** hereinafter.

11. As to Claim 21, reasons are included in **[Response A]** and **[Response B]** given above.

Allowable Subject Matter

12. Claims 3 – 9, 13 and 15 – 20 are objected to as being dependent upon a rejected base claim, but they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed because the prior art does not teach or fairly suggest the following subject matter:

- A method/control apparatus for operating semiconductor chips arranged in groups on modules comprising *selecting a group of semiconductor chips from the semiconductor chips on the modules based on a prescribed selection criterion for selecting a group of semiconductor chips based on a temperature of the semiconductor chips* in combination with other limitations as recited in **Claim 3** and **Claim 15**, respectively;
- A method/control apparatus for operating semiconductor chips arranged in groups on modules comprising *selecting a group of semiconductor chips from the semiconductor chips on the modules using a statistical method* in combination with other limitations as recited in **Claim 4** and **Claim 16**, respectively;
- A method for operating semiconductor chips arranged in groups on modules wherein *each of the semiconductor chips has an associated election probability* in combination with other limitations as recited in **Claim 7**;
- A control apparatus for operating semiconductor chips arranged in groups on modules comprising *a selection device for assigning each semiconductor chip an individual election probability* in combination with other limitations as recited in **Claim 17**;
- A control apparatus for operating semiconductor chips arranged in groups on modules comprising *an assessment device* in combination with other limitations as recited in **Claim 18**;
- A method/control apparatus for operating semiconductor chips arranged in groups on modules wherein *each of the semiconductor chips has an associated individual index which denotes a corresponding module and a position of a corresponding semiconductor chip on the corresponding module* in combination with other limitations as recited in **Claim 9** and **Claim 19**, respectively;
- A method for operating semiconductor chips arranged in groups on modules wherein, *beside the group of semiconductor chips which is selected in method step a), a further group of further semiconductor chips is selected independently of module, wherein data exchange between data lines in a common data bus and the semiconductor chips in a group selected in method step c) involves*

alternating between groups of semiconductor chips in combination with other limitations as recited in **Claim 13**;

- A control apparatus for operating semiconductor chips arranged in groups on modules comprising *a register device for storing information about an association between the semiconductor chips and an active group of semiconductor chips* in combination with other limitations as recited in **Claim 20**.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J Lin whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272 - 1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
March 20, 2005